IN THE UNITED STATES PATENT OFFICE

Appellants:	Philip B. James-Roxby et al.		
Assignee:	Xilinx, Inc.		
Title:	Method and Apparatus for Multithreading on a Programmable Logic Device		
Serial No.:	10/769,330	File Date:	January 30, 2004
Examiner:	Abdou K. Seye	Art Unit:	2194
Docket No.:	X-1557-2 US	Conf. No.:	7401

PRE-APPEAL CONFERENCE BRIEF

Dear Sir:

This Brief is submitted for the Pre-appeal Conference requested in the Notice of Appeal with which this Brief is submitted.

A. The rejection of claims 1-20 should be reversed, because the Examiner has not established a *prima facie* case of obviousness of the claims under 35 U.S.C. §103(a) over "He" in view of "Ohnishi".

The Examiner stated that He teaches configuring configurable logic of an IC to have a plurality of thread circuits. (Final Office Action, p. 3). The Examiner cited in part paragraph 0023 of He, which states that "[i]n one embodiment, at least a first part of the IC design is interconnected on at least a first thread [and] [a]t least a second part of the IC design is interconnected on at least a second thread." After review of He in its entirety, it is clear that He's reference to "threads" is different from Appellants' "thread circuits." In particular, He describes a routing algorithm implemented in software on a computer that can be multi-threaded or single-threaded. (See He, para. 0009). That is, the software that implements the router can be multi-threaded. He is not referring to "thread circuits" implemented in configurable logic of an IC. See also He, para. 0037 ("In addition, since the routing task has been divided, multi-threaded parallelism can be applied to speed up the global router 201," and "[t]he detail router 202 can route these areas in parallel utilizing the multi-threaded parallel computing capability of some embodiments of the present invention."), para. 0046 ("Some embodiments use the multi-threaded mechanism provided by the computer operating

system to route all, or multiple, areas in parallel."), and para. 0047 ("FIG. 5 depicts an embodiment of the area-oriented, multi-threaded graph-based detail router 500."). Thus, it is clear that the "threads" in He do not teach or suggest "thread circuits," as recited in Appellants' claims.

In the Advisory Action, the Examiner stated that He teaches an IC design including parts and that each part is associated with a thread. (citing He, para. 0024). The cited paragraph 0024, however, does not recite such a teaching. Rather, paragraph 0024 of He states that the software router can be implemented in hardware parts, such as an IC or computer. The Examiner also cited a multi-level global routing grid in FIG. 4 of He, paragraphs 0039-0043. FIG. 4 in He is related to the algorithm used to route a design, and not to a design having thread circuits. Finally, Applicants have performed a word search of the text of He with respect to the term "thread" and have found no instances of the term "thread' being used in conjunction with a circuit or the like in an IC design. The Examiner has incorrectly interpreted "thread" as it is used in He.

The Examiner also cited "interconnections" in He as teaching Appellants' "interconnect topology" among thread circuits. (Final Office Action, p. 3). The "interconnections" in He refer to physical routing in an IC produced by the router. See He, para. 0006, 0022. These generic interconnections in He do not teach a specific interconnection topology among a plurality of thread circuits, as recited in Appellants' claim 1.

In the Advisory Action, the Examiner stated that He teaches interconnections between objects/parts/cells in an IC. (citing He, para. 0013; FIG. 4). However, object/parts/cells in He do not teach or suggest thread circuits. Thus, the cited interconnections cannot logically teach or suggest an interconnection topology among thread circuits.

Thus, while He uses similar language to Appellants' claims, it is apparent from the citations above that He is actually referring to traditional multi-threaded software, and not to an IC with thread circuits. Ohnishi generally teaches a logic synthesis process for circuit design. (Ohnishi, Abstract). Ohnishi does not teach or suggest configuring configurable logic of an IC to have a plurality of thread circuits and an

interconnection topology among the thread circuits, as recited in Appellants' claim 1. Since neither He nor Ohnishi teach or suggest such features, no permissible combination thereof renders obvious Appellants' invention recited in claim 1.

Further, "rejections on obviousness cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." KSR Int'l Co. v. Teleflex, Inc. 82 USPQ.2d 1385, 1396 (S. Ct. 2007). There is no suggestion, motivation, or other objective reason to modify He with thread circuitry described in Ohnishi. He describes multi-threaded software for routing designs in an IC. There is no want, need, motivation, or otherwise for modifying He in order to implement specific thread circuitry in an IC. The Examiner's proposed reason for the combination of improving the efficiency of He's system is not applicable, since He does not disclose thread circuitry to which such efficiencies can be applied. Thus, a prima facie case of obviousness has not been established.

Appellants' independent claims 7, 14, and 18 each recite features similar to those emphasized above in claim 1. For the same reasons, the cited combination does not render obvious Appellants' claims 7, 14, and 18. Claims 2-6, 8-13, 15-17, and 19-20 depend from claims 1, 7, 14, and 18 and recite additional features thereof. Since the cited combination does not render obvious Appellants' invention recited in claims 1, 7, 14, and 18, the cited combination also fails to render obvious Appellants' invention recited in claims 2-6, 8-13, 15-17, and 19-20.

Accordingly, Appellants contend that claims 1-20 are patentable over the cited combination and fully satisfy the requirements of 35 U.S.C. §103. Appellants respectfully request that the present rejection be reversed.

Conclusion

In view of the above, Appellants submit that the rejections are improper, the claimed invention is patentable, and that the rejections of claims 1-20 should be

reversed. Appellants respectfully request reversal of the rejections as applied to the appealed claims and allowance of the entire application.

I hereby certify that this correspondence is being filed via EFS-Web with the United States Patent & Trademark Office on September 8, 2009.

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Respectfully submitted,

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